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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,901	06/23/2000	James R. Peterson	500689.01	9313

27076 7590 06/05/2003

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	7

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/602,901	PETERSON ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-39* is/are pending in the application.

4a) Of the above claim(s) *1,8,14,19,26 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13,15-18,20-25,27-30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 30 recites the limitation "the computer system of claim 26". There is insufficient antecedent basis for this limitation in the claim. Claim 26 has been cancelled. The examiner assumes claim 30 is dependent upon claim 28.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-7, 9-13, 15-18, 32-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox (U.S. Patent No. 5,357,621 in view of Helm et al. (U.S. Patent No. 5,129,069).

Referring to claims 4, 10, 16, 35, 37, Cox teaches an expandable memory system for use in a computing system which comprises a plurality of plug-in memory modules coupled to a memory system controller in a serial network. The memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory

system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers (col. 2, lines 36-50). The expandable memory system utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells (memory sub-array) (col. 2, lines 53-59, also with reference to Fig. 1). The system also includes the capability to bypass or disable bad memory modules and reassign memory addresses without leaving useable memory unallocated (col. 3, lines 37-39). As shown in Fig. 1, the memory modules are linked together through bus 19 a-c. If the physical address falls within the range of the addressable memory of a memory module (i.e. base address + size), then the memory module is enabled and memory accesses are allowed via the system DRAM controller 33 as shown in Fig. 2 (col. 5, lines 51-54). Cox further teaches undefined blocks or space may be left in the memory space if necessary, for example, to bypass a failed memory block (col. 5, lines 31-33). Thus, it is implied that the memory module 20 can keep track of the number of all the functional memory blocks.

Thus, Cox teaches all the limitations of claims 4, 10, 16, except for that the memory module controllers do not directly access memory requests.

However, Helm et al. teach a memory apparatus for a computer which includes: a memory unit having a storage section which includes a plurality of addressable storage locations; and an address decoding arrangement for determining whether a computer memory address output by the computer to which the memory unit is detachably electrically coupled is within a

range of consecutive addresses, the address decoding arrangement including a base address register, a size register, and an arrangement for facilitating loading of first and second values respectively into the base address and size registers from a computer to which the memory unit is detachably electrically coupled, the first value defining a memory address in the predetermined range and the second value defining the number of addresses in the range, the storage section including an arrangement responsive to detection by the address decoding arrangement that a computer memory address is within such range for facilitating access to a corresponding one of the plural storage locations by the computer (col. 1, lines 58-68, and col. 2, lines 1-11). As shown in Figs. 1 and 2, Helm et al. teaches the memory control signals 16 provide an indication to memory devices when a memory access cycle is in progress, include signals which indicate whether the addressed memory location is to be read or written, and may include additional signals required by different types of conventional memory devices to facilitate proper timing of data transfers (col. 3, lines 32-38). Thus, each memory module can access memory requests from the CPU 11.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Helm et al. in combination with the memory system as taught by Cox in order to provide an automatic memory configuration in a manner which is highly efficient and yet involves minimal hardware cost (col. 1, lines 52-55).

In regard to claims 2, 9, 15, 17, 34, as shown in Fig. 2, Cox teaches each memory block (23, 25, 27, 29) comprising, for example, a 256 k-byte dynamic random access memory (DRAM) array (col. 4, lines 21-26), embedded in the memory modules 1-n.

Referring to claims 3, 5, 11, 18, 32-33, and 39, as cited above, Cox teaches undefined blocks or space may be left in the memory space if necessary, for example, to bypass a failed memory block (col. 5, lines 31-33). Cox further teaches the Memory Address Mask command (Opcode 40-4F) is utilized to assign the base address for the first memory module on the control link. The mask value corresponds to the upper 4 bits of actual addresses in a 16 megabyte memory system where a 1-megabyte block of memory equals 1 mask value. The mask command values range from 40 to 4F. The 0 to F hexadecimal values define the absolute starting block address in increments of 1 megabyte per block. If more than 1 megabyte of memory exists on a given memory module, the MCL controller 22 will sequentially build additional addressing for each additional block of 1 megabyte of memory (col. 10, lines 1-13). Thus, Opcode 40-4F is used to keep track of the number of functional sub-arrays in the memory module.

Referring to claims 6 and 12, Cox teaches upon power up, the memory system controller automatically configures the memory system assigning an address to each of the memory module controllers in the network and a base address for the memory on each of the memory modules in the system (col. 2, lines 65-68, and col. 3, lines 1-2).

In regard to claims 7, 13, 36, 38, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module. The process is repeated for each memory module 20 in turn until the entire memory space is defined. The starting addresses that are assigned to each of the individual memory modules 20 are referred to as base addresses. A

specific memory module 20 will respond to addresses defined from [BASE] to [BASE+SIZE] (col. 5, lines 33-43).

5. Claims 20-25, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (U.S. Patent No. 6,252,612) in view of Cox (U.S. Patent No. 5,357,621), and further in view of Helm et al. (U.S. Patent No. 5,129,069).

Referring to claims 22 and 28, Jeddeloh teaches a computer, comprising at least one processor; and at least two memory controllers, wherein one of the at least two memory controllers includes an accelerated graphics port and at least one configuration register defining a range of addresses that are available for accelerated graphics port transactions (col. 3, lines 36-42). As shown in Fig. 2, Jeddeloh teaches the computer 150 includes at least one processor 152 connected to a first memory controller 154 and a second memory controller 155 by a processor or host bus. The computer 150 also has a first main memory 156 and a second main memory 157 connected to the first memory controller 154 and the second memory controller 155, respectively. A graphics accelerator 160 communicates with a local frame buffer 162 and the first memory controller 154 through an accelerated graphics port (AGP) 166. The AGP 166 is a point-to-point connection between the first memory controller 154 and the graphics accelerator 160. The first memory controller 154 and the second memory controller 155 also accept memory requests from a PCI bus 158 (col. 4, lines 5-26). It is inherent that the computer system of Jeddeloh comprises a system processor and system bus.

Thus, Jeddeloh teaches all the limitations of claims 22 and 28 except that the first memory and the second memory are segmented into plurality of memory sub-arrays, and the first

memory controller and the second memory controller coupled to the memory request to receive memory access requests.

However, as cited above, Cox teaches a memory system comprising a plurality of memory modules, each comprising a memory controller, and a memory segmented into plurality of memory blocks.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox in combination with the computer system as taught by Jeddeloh in order to control the expandable memory without user intervention and without leaving useable memory unallocated (col. 3, lines 28-40).

Thus, Jeddeloh and Cox teach all the limitations of claims 22 and 28 except that the memory controller directly access memory requests.

However, as cited above, Helm et al. teach a memory system with plurality of memory module, each comprising a memory controller directly accessing memory requests.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Helm et al. in combination with the memory system as taught by Jeddeloh and Cox in order to provide an automatic memory configuration in a manner which is highly efficient and yet involves minimal hardware cost (col. 1, lines 52-55).

Referring to claims 20, 27, and 29, although Jeddeloh does not teach the first memory array comprising an embedded memory array, as cited above, Cox teaches each memory block (23, 25, 27, 29, see Fig. 2) comprising, for example, a 256 k-byte dynamic random access memory (DRAM) array (col. 4, lines 21-26), embedded in the memory modules 1-n.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox in combination with the computer system as taught by Jeddeloh in order to control the expandable memory without user intervention and without leaving useable memory unallocated (col. 3, lines 28-40).

Referring to claims 21, 23, and 30, although Jeddeloh does not teach the register of the memory controller to store a pointer value for each of the functional memory sub-arrays, as cited above, Cox teaches undefined blocks or space may be left in the memory space if necessary, for example, to bypass a failed memory block (col. 5, lines 31-33). Cox further teaches a register is used to keep track of the number of functional sub-arrays in the memory module.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox in combination with the computer system as taught by Jeddeloh in order to control the expandable memory without user intervention and without leaving useable memory unallocated (col. 3, lines 28-40).

In regard to claims 24 and 25, although Jeddeloh does not teach storing a start address and size value for the first and second memory array, and the start value stored by the second memory controller is the sum of the start value and the size value stored by the first memory controller.

However, as cited above, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module. The process is repeated for each memory module 20 in turn until the entire memory space is defined. The starting addresses that are assigned to each of the individual memory modules 20 are referred to as base addresses. A

specific memory module 20 will respond to addresses defined from [BASE] to [BASE+SIZE] (col. 5, lines 33-43).

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox in combination with the computer system as taught by Jeddeloh in order to control the expandable memory without user intervention and without leaving useable memory unallocated (col. 3, lines 28-40).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

05/29/2003

Matthew C. Bella

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